MONTGOMERY COLLEGE, ROCKVILLE  
Physics, Engineering and Geosciences Department  
EE 244 – Digital Logic Design  
Fall 2008  

Practice Midterm

1. (3) Convert the following unsigned integer to decimal: 110011001100

   \[110011001100 = 4 + 8 + 64 + 128 + 1024 + 2048 = 3276\]

2. (3) Convert the following decimal number to hexadecimal: 791

   We first convert to binary:
   
   \[
   \begin{align*}
   791 / 2 &= 395 \quad \text{rem} \ 1 \\
   395 / 2 &= 197 \quad \text{rem} \ 1 \\
   197 / 2 &= 98 \quad \text{rem} \ 1 \\
   98 / 2 &= 49 \quad \text{rem} \ 0 \\
   49 / 2 &= 24 \quad \text{rem} \ 1 \\
   24 / 2 &= 12 \quad \text{rem} \ 0 \\
   12 / 10 &= 110 \quad \text{rem} \ 0 \\
   1 / 8 &= 0 \quad \text{rem} \ 1
   \end{align*}
   \]

   Adding leading 0's we get 0011 0001 0111 = 317_{16}

3. (4) The following decimal integers are to be stored in a 6-bit two’s complement format. Show how they are stored.
   a. +32
   b. -32
   c. -16
   
   +32: cannot be stored (It would need another bit.)
   -32: 100000
   -16: 110000

4. (7) In IEEE standard 32-bit notation, how would the following decimal be stored? -48.5

   \[48.5 \Rightarrow 110000.1000000 = 1.10000100000000000 \times 2^5\]
   \[\Rightarrow 1 10001000 10000000000000000\]

5. (8) Reduce the expression to a minimum SOP form, using P1 through P12.
   \[h = ab' + bc'd' + abc'd + bc\] (3 terms, 5 literals)

   \[h = a b' + b c' d' + a b c' d + b c\]
   \[= a b' + b c' d' + a b c' + b c\]
   \[= a b' + b c' d' + a b + b c\]
   \[= a b' + b c' d' + b c\]
   \[= a + b d' + b c\]
   \[\text{or}\]
   
   \[h = a b' + b c' d' + a b c' d + b c\]
   \[= a b' + b c' d' + a b d + b c\]
   \[= a b' + b d' + a b d + b c\]
   \[= a b' + b d' + a b + b c\]
   \[= a + b d' + b c\]

6. (25) For the following circuit:
a. Compute the maximum delay,
   i. Assuming that all inputs are available both uncomplemented and complemented = 6Δ
   ii. Assuming only uncomplemented inputs are available, and an additional gate must be added to complement each input = 6Δ
b. Compute the maximum delay from input D to the output, assuming only uncomplemented inputs are available, and an additional gate must be added to complement each input = 5Δ

7. (25) Design a priority encoder with seven active low inputs, p1', . . . , p7' and three active high outputs, CBA that indicate which is the highest priority line active is designed using AND, OR, and NOT gates. Input p1' is highest priority; p7' is lowest. If none of the inputs are active, the output is 000. Assume that is a fourth output line, M, which is 1 if there are multiple active inputs. Show the truth table and Boolean expressions for C, B and A.

<table>
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<tr>
<th>p1'</th>
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<th>p3'</th>
<th>p4'</th>
<th>p5'</th>
<th>p6'</th>
<th>p7'</th>
<th>C</th>
<th>B</th>
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C = p1' p2' p3' (p4' ' + p5' ' + p6' ' + p7' ')
B = p1' (p2' ' + p3' ') + p1' p4' p5' (p6' ' + p7' ')
A = p1' ' + p2' p3' ' + p2' p4' p5' ' + p2' p4' p6' p7' '

8. (25) For the following set of functions, design a system using
a. a ROM (show the circuit)

b. a PLA with 6 product terms (show Karnaugh maps, the algebraic expressions, as well as the PLA circuit)

c. a PAL (show Karnaugh maps, the algebraic expressions, as well as the PAL circuit)

\[ f(a,b,c,d) = \Sigma m(3,5,6,7,8,11,13,14,15) \]

\[ g(a,b,c,d) = \Sigma m(0,1,5,6,8,9,11,13,14) \]